M65810FP

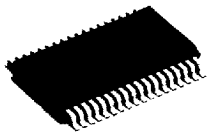
DIGITAL AUDIO INTERFACE RECEIVER

DESCRIPTION

The M65810FP is a semiconductor IC for receiving and decoding digital audio data conforming to the EIAJ (CP-340) standards, transmitted from digital audio equipment such as CD, DAT, DCC, and MD players and BS tuner. It has substantial functions such as built-in input selectors for 6 channels and PLL containing VCO. Furthermore, the IC can read information allotted to serial copy management systems.

FEATURES

- A total of 6 channels of selectable inputs : 3 channels of optical inputs (CMOS level) and 3 channels of coaxial cable inputs (with a built-in converter to change minimum of 400mV$_{PP}$ into CMOS level) (Selected input is output at the feedthrough pin)
- Two kinds of control modes, microcomputer mode using serial data and easy mode using parallel data, are available to choose from as input selection
- Built-in PLL circuit containing VCO
- Selection of master clock from 384fs and 256fs
  Equipped also with dedicated 128fs output pin
- If an error occurs on parity check, the preceding value in audio data is held to prevent noise
- If PLL is unlocked, digital audio data is set to "all 0"to mute
- U and V bits are output at dedicated pins (in micro computer mode)
- Word clock output pin gives capability of dealing with diverse kinds of DA converter ICs



Outline 36P2R-A

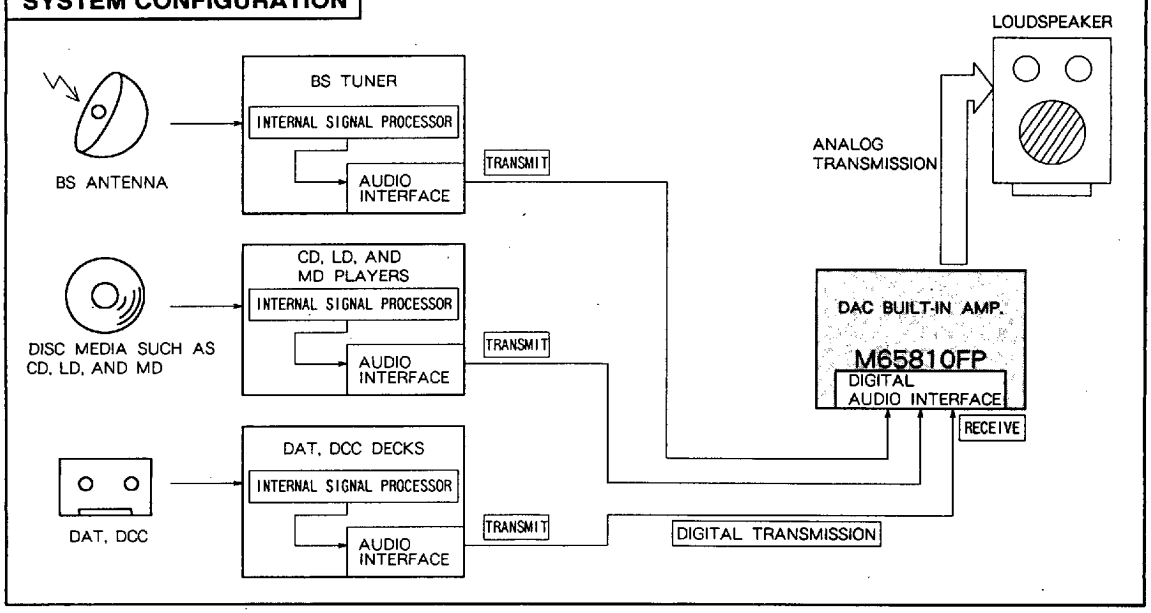
0.8mm pitch 450mil SSOP
(8.4mm × 15.0mm × 2.0mm)

- Outputs C-bit fs information and emphasis information at dedicated pins. The first 32 bits in C-bit data can be read in serial data from in microcomputer mode

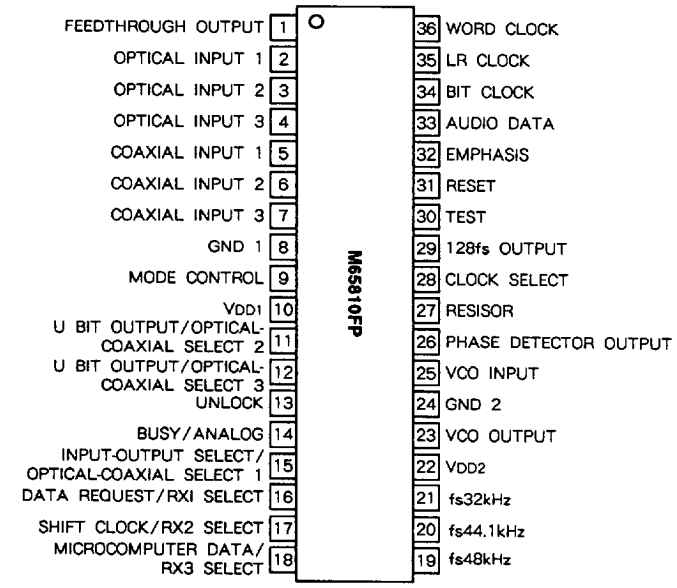
RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... V_{DD} = 4.75 to 5.25V
Rated supply voltage ..... V_{DD} = 5V

SYSTEM CONFIGURATION

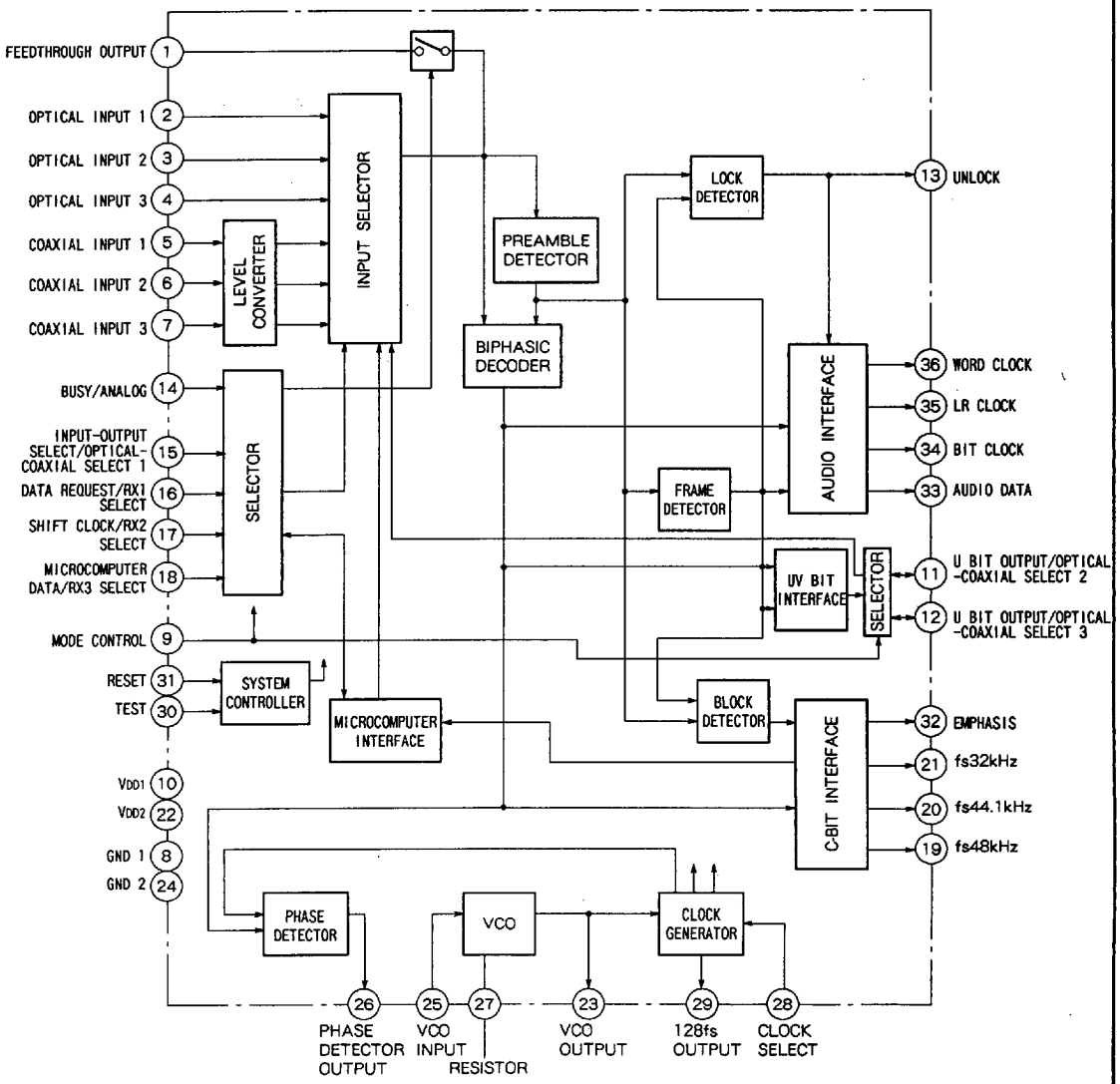


PIN CONFIGURATION (TOP VIEW)



Outline 36P2R-A

IC INERNAL BLOCK DIAGRAM



PIN DESCRIPTION (I↓ denotes input with pull-down resistor)

Pin No.	Symbol	Name	I/O	Usage
①	FTO	Feedthrough output	O	Through output of selected RX
②	ORX1	Optical input 1	I	CMOS level inputs
③	ORX2	Optical input 2	I	
④	ORX3	Optical input 3	I	
⑤	CRX1	Coaxial input 1	I	Inputs to internal level converter Minimum input voltage 400mV$_{P-P}$
⑥	CRX2	Coaxial input 2	I	
⑦	CRX3	Coaxial input 3	I	
⑧	VSS1	GND 1	–	
⑨	MODE	Mode control	I	H = microcomputer mode, L = easy mode
⑩	V_{DD1}	V_{DD1}	–	
⑪	UBO/ OCSEL2	U bit output/optical-coaxial select 2	O I	In microcomputer mode:U-bit data output(in synchronization with LRCK) In easy mode : RX1 optical line/coaxial line input selector, H = optical line input
⑫	VBO/ OCSEL3	U bit output/optical-coaxial select 3	O I	In microcomputer mode:V-bit data output(in synchronization with LRCK) In easy mode : RX2 optical line/coaxial line input selector, H = optical line input
⑬	UNLOCK	Unlock	O	PLL unlock information : unlock = H
⑭	BUSY/ANALOG	Busy/analog	O I↓/O	In microcomputer mode:modification information about C-bit data contents, modefication=H In easy mode:RX inputs are all shout off on a H pulse and VCO also stops
⑮	IOSEL/OCSEL1	Input-output select/ optical-coaxial select 1	I I	In microcomputer mode:data input/output selector, H=microcomputer→DAI, L=DAI→microcomputer In easy mode:RX3 optical line/coaxial line input selector, H=optical line input
⑯	REQ/ RX1SEL	Data request/ RX1 select	I↓ I↓/O	In microcomputer mode : data input/output enabled at H In easy mode : RX1 is selected on H pulse and H is held
⑰	SCK/ RX2SEL	Shift clock/ RX2 select	I↓ I↓/O	In microcomputer mode : data is shifted on a fall In easy mode : RX2 is selected on H pulse and H is held
⑱	MDATA/ RX3SEL	Microcomputer data/ RX3 select	I↓/O I↓/O	In microcomputer mode : serial data input/output In easy mode : RX3 selected on H pulse and H is held
⑲	FS48	fs48kHz	O	Set by C-bit fs code : 48kHz = L
⑳	FS44	fs44.1kHz	O	Set by C-bit fs code : 44.1kHz = L
㉑	FS32	fs32kHz	O	Set by C-bit fs code : 32kHz = L
				These are all set to H under unlock condition.
㉒	V_{DD2}	V_{DD2}	–	Power supply to VCO
㉓	VCOO	VCO output	O	=384fs or 256fs(according to the polarity of pin ㉘)master clock output
㉔	VSS2	GND 2	–	Ground of VCO. Same voltage as VSS1.
㉕	VCOI	VCO input	I	VCO control voltage input
㉖	PDO	Phase detector output	O	Forms an external loop filter
㉗	R1	Resistor	–	Adusts free-running oscillation frequency by resistor for adjustment of VCO oscillation frequency
㉘	CKSEL	Clock select	I	Master clock frequency selector : H = 384fs, L = 256fs
㉙	128FS	128fs output	O	128fs clock output
㉚	TEST	Test	I	Test pin. Normally fixed to L, TEST = H
㉛	$\overline{\text{RESET}}$	Reset	I	Initialization at power up. RESET = L
㉜	EMP	Emphasis	O	Set by C-bit emphasis code : 50/15 μ sec = H
㉝	ADATA	Audio data	O	16-bit audio data serial output (MSB first)
㉞	BCK	Bit clock	O	Audio data shift clock = 64fs
㉟	LRCK	LR clock	O	= fs
㊱	WCK	Word clock	O	= 2fs (50% duty)

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DD}-V_{SS}$	Suply voltage	− 0.3 to 6.5	V
$V_{DD1}-V_{DD2}$	Voltage difference between VDD 1 and 2.	± 0.3	V
V_I	Input voltage	V_{SS} − 0.3 to V_{DD} + 0.3	V
P_d	Power dissipation	1100	mW
T_{opr}	Operating temerature	− 20 to + 70	℃
T_{stg}	Storage temperature	− 40 to + 125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Suplly voltage		4.75	−	5.25	V
V_{IH}	Input voltage (H level)		0.7V_{DD}	−	V_{DD}	V
V_{IL}	Input voltage (L level)		V_{SS}	−	0.3V_{DD}	V
fvco	Oscillation frequency (VCO)	CKSEL = L	−	256fs	−	−
fvco	Oscillation frequency (VCO)	CKSEL = H	−	384fs	−	−
fs	Input signal sampling frequency		32	−	48	kHz

ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{DD}	Circuit current	When receiving fs = 44.1kHz	−	20	−	mA
V_{OH}	Output voltage (H level)	I_{OH} = − 500 μA	$V_{DD}-1$	−	−	V
V_{OL}	Output voltage (L level)	I_{OL} = 500 μA	−	−	0.4	V
I_{IN}	Input leak current	$V_I = V_{SS} \sim V_{DD}$	−	−	± 1	μA
I_{OL}	Driver current	V_{OL} = 0.5V, pins ⑲⑳㉑	15	−	−	mA
I_{OH}	Driver current	$V_{OH} = V_{DD}$ − 1.5V, pins ⑭⑯⑰⑱	15	−	−	mA
R_{ID}	Input pull-down resistance	Pins ⑭⑯⑰⑱	20	−	100	kΩ

FUNCTION DESCRIPTION

6 channel input selector

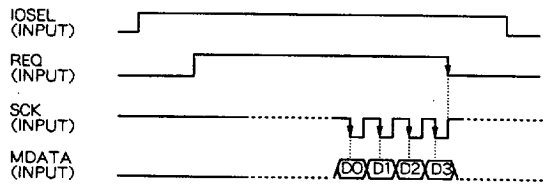
1. Easy mode (MODE=L)

Input		OCSEL 1	OCSEL 2	OCSEL 3	RX1SEL	RX2SEL	RX3SEL	ANALOG
Optical input	ORX1	H	–	–	⌐¬	–	–	–
	ORX2	–	H	–	–	⌐¬	–	–
	ORX3	–	–	H	–	–	⌐¬	–
Coaxial input	CRX1	L	–	–	⌐¬	–	–	–
	CRX2	–	L	–	–	⌐¬	–	–
	CRX3	–	–	L	–	–	⌐¬	–
Analog mode		–	–	–	–	–	–	⌐¬

- RX inputs are selected at the positive-going edge of a H pulse inputted to the RX1SEL to RX3SEL pins. As the H level is held therefrom, they can be used for indicator lamps and the like.
- If a H pulse is inputted to the ANALOG pin, the analog mode takes place at the positive-boing edge of the H pulse. None of RX inputs are acceped and VCO stops.
- If a H pulse is inputted to RX1SEL to RX3SEL in analog mode, a predetermined RX input is selected at the positive-going edge of the H pulse, and VCO oscillation starts.

2. Microcomputer mode (MODE=H)

In microcomputer mode, it is possible to select RX inputs during input mode (IOSEL = H : microcomputer→DAI)



Data is taken into the IC at the negative-going edge of SCK, and then is latched at the negative-going edge of REQ. According to the last 4 bits, selection of RX inputs and control of feedthrough output are carried out.

Input		D1	D2	D3
Optical input	ORX1	H	H	H
	ORX2		H	L
	ORX3		L	H
Coaxial input	CRX1	L	H	H
	CRX2		H	L
	CRX3		L	H
Analog mode		X	L	L

None of RX inputs are accepted and VCO stops in analog mode.

The feedthrough output (FTO) is turned ON/OFF by the polarity of DO.

DO	FTO
L	ON
H	OFF (fixed to L)

3. Input signal voltage range

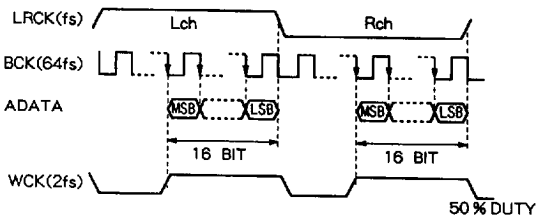
Optical input (ORX1 to 3)		Coaxial input (CRX1 to 3)	
L level	H level	Min	Max
$0.3V_{DDmax}$	$0.7V_{DDmin}$	$400mV_{P-P}$	$5V_{P-P}$

Audio Interface

1. Audio format

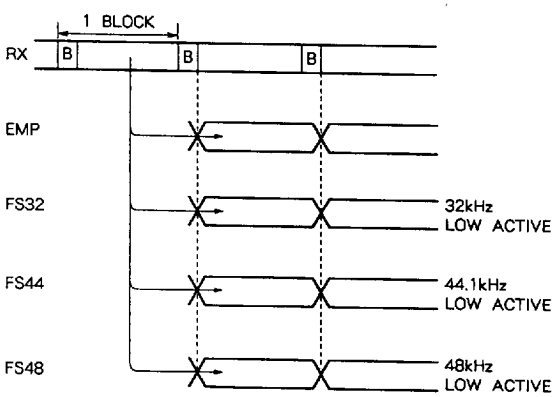
MSB first, last 16 bit

2. Audio data output timing



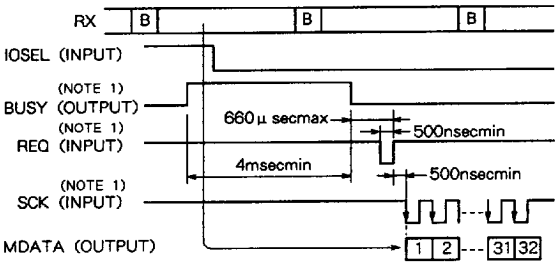
C-Bit data output timing

1. Output through dedicated pins



2.Serial data output in microcomputer mode (MODE=H)

In microcomputer mode, it is possible to read out the first 32 bits in C-bit data during output mode (IOSEL = L : DAI→ microcomputer)

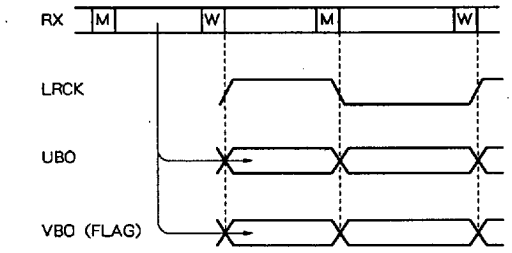


Note 1.BUSY gose high if the first 32 bits in C-bit data change, compared with the previous block. It gose back low if consecutive 2 blocks consist of the same content.
Consequently, the minimum H pulse width of BUSY is 4ms (when fs = 48kHz).
If BUSY gose high, read out C-bit data after detecting the negative-going edge of BUSY because new contents of C-bit data transferred to the output register are the beginning of the next block.

Note 2. As the first 32 bits in C-bit data are loaded to the output register at the inverting edge of REQ, be sure to invent REQ before reading out C-bit data. SCK is taken into the IC only when REQ is high, so that REQ should be constantly retained high while reading.
As BUSY compulsively goes back low at the inverting edge of REQ, let REQ go high within 660 μs (the shortest time at which BUSY may go high next) after a fall of BUSY so as to make sure that next BUSY is detected.
If it is impossible to meet the 660μs requirement due to the timer a microcomputer has, it is recommended to use both kinds of operation, to read with BUSY and to read C-bit data periodically (every several milliseconds to several tens of milliseconds) independently of BUSY.

Note 3. To read out C-bit data, set SCK to high level at the positive-going edge of REQ.

U-Bit/V-bit data output timing



Reset

By resetting after power up, it is possible to arrange the following initial settings.

1. In easy mode

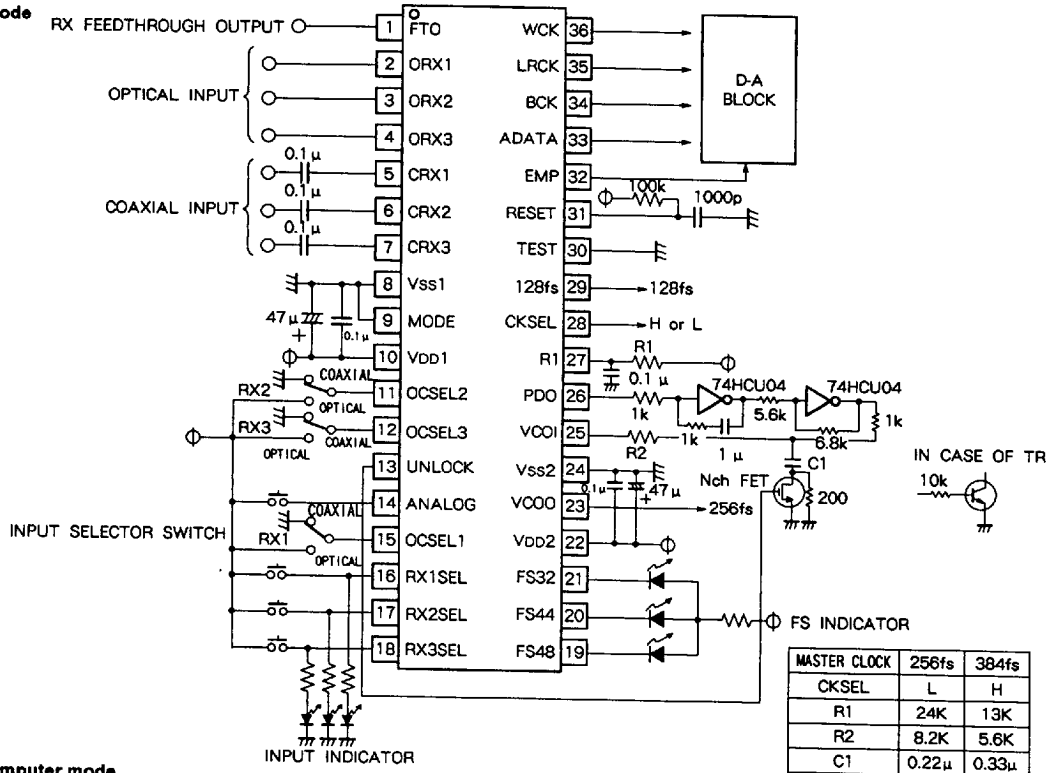
The RX1 input is selected. Optical/coaxial lines are selected by the polarity of OCSEL 1 to 3.

2. In microcomputer mode

The ORX1 (optical line) input is selected.

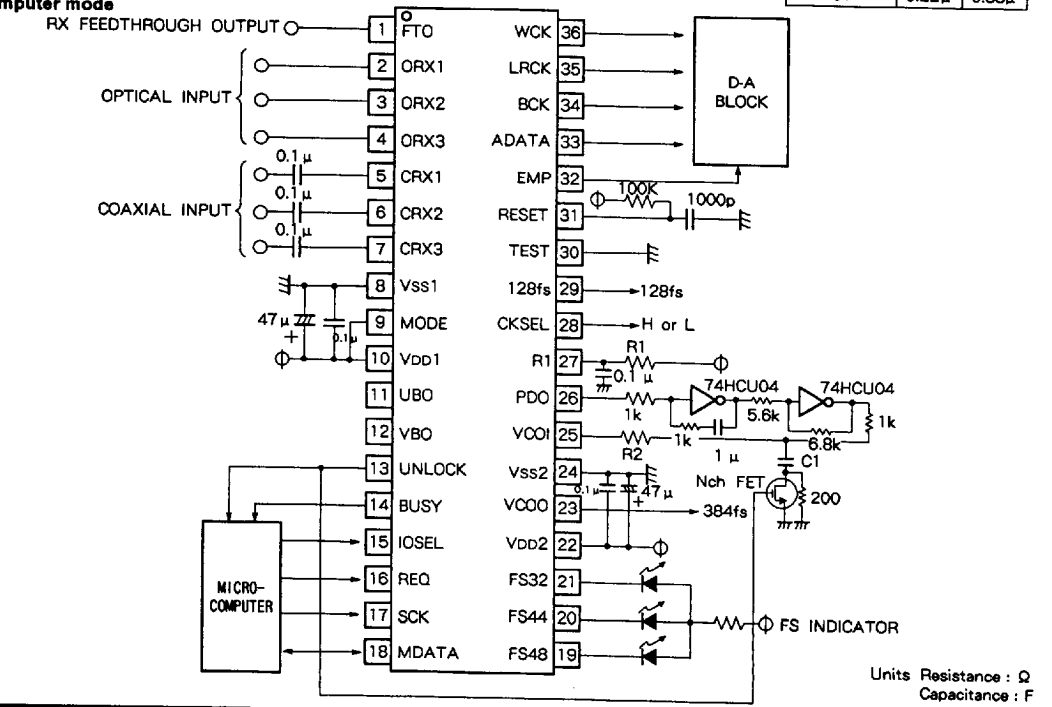
APPLICATION EXAMPLE

1) Easy mode



MASTER CLOCK	256fs	384fs
CKSEL	L	H
R1	24K	13K
R2	8.2K	5.6K
C1	0.22µ	0.33µ

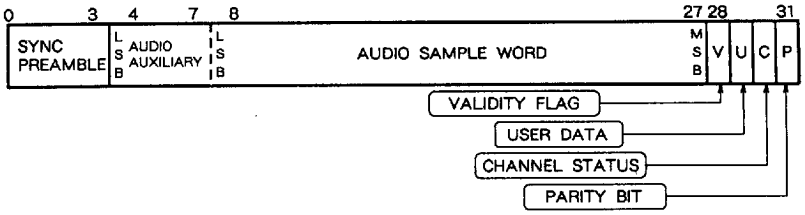
2) Microcomputer mode



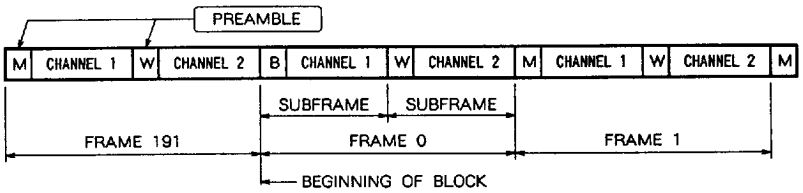
Units Resistance : Ω
Capacitance : F

EIAJ STANDARD FORMAT

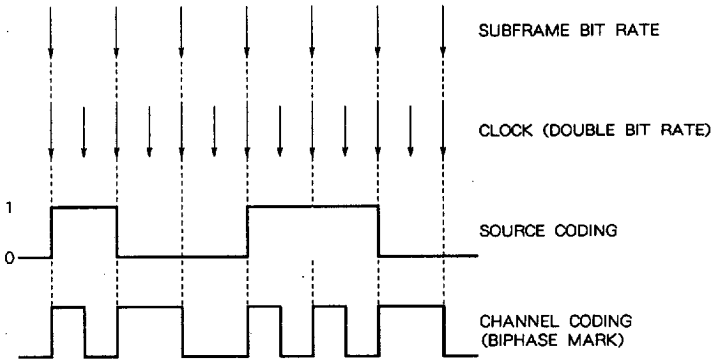
(Fig. 1)
Subframe format



(Fig. 2)
Frame format



(Fig. 3)
Biphasic mark system



(Table 1) Preamble channel coding

Preamble	Channel coding	
	Precedence symblol : 0	Precedence symblol : 1
"B"	11101000	00010111
"M"	11100010	00011101
"W"	11100100	00011011

(Fig. 4)
Preamble "M"